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| EXAMINER | |
| --- | --- |
| CAMPOS, YAIMA | |
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| 2185 | |

| SHORTENED STATUTORY PERIOD OF RESPONSE | MAIL DATE | DELIVERY MODE |
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

| Office Action Summary | Application No. 10/828,677 | Applicant(s) AHRENS ET AL. | |
|---|---|---|---|
| | Examiner Yaima Campos | Art Unit 2185 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on _31 October 2006_.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) _1-11 and 13-22_ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _1-11 and 13-22_ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## RESPONSE TO AMENDMENT

1. The examiner acknowledges the applicant's submission of the amendment dated October 31, 2006. At this point claims 1-2, 4, 10-11, 13 and 20-22 have been amended and claim 12 has been cancelled. There are 21 claims pending in the application; there are 4 independent claims and 17 dependent claims, all of which are ready for examination by the examiner.

## I. <u>REJECTIONS BASED ON PRIOR ART</u>

### <u>*Claim Rejections - 35 USC § 103*</u>

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. <u>**Claims 1-11 and 13-22**</u> are rejected under 35 U.S.C. 103(a) as being unpatentable over Talangala et al. (US 2002/0161972) in view of Dalal et al. (US 2004/0123063) and Lu et al. (Us 2004/0225834).

3. As per <u>**claims 1, 13 and 21-22**</u>, Talangala discloses

"A method/system/network system having a plurality of nodes for dynamic striping, comprising:" as **["dynamic striping may be employed so that new writes form new parity group. Thus, stripes of various sizes may be supported by the storage system" (Column 2, paragraph 0012)]**

"software instructions stored in the memory for enabling the under control of the processor, to:" **[With respect to this limitation, Talangala discloses "To facilitate keeping track of the data and parity information, a block remapping technique may be implemented in software and/or hardware which maps a logical or virtual block address to a physical storage device segment" (Column 6, paragraph 0054 and Column 3, paragraph 0033, lines 21-26)]**

"receiving a request to write a **first** data block into a storage pool;" **[With respect to this limitation, Talangala discloses "receiving a write transaction specifying the virtual addresses of a subset of the data blocks of a data stripe" (Column 3, paragraph 0017 and Column 6, paragraph 0059)]**

"determining a physical disk location in the storage pool to store the **first** data block using a dynamic striping policy, **wherein the dynamic striping policy comprises at least one selected from the group consisting of a dynamic striping policy based on physical disk speed, a dynamic striping policy based on free space available on physical disks, a dynamic striping policy based on load on physical disks, and a round robin policy**;" **[With respect to this limitation, Talangala discloses that "With dynamic striping, the host machine interacts with the storage array via virtual addresses" and explains that "When a block is written, a physical location is chosen for it" (Column 6, paragraph 0059). Talangala also discloses having a "free segment bitmap" used to "keep track of all physical segments on all storage devices" to allocate new data to free/empty segments (Column 5, paragraph 0051). Talagala also explains "when processor 100 of FIG. 1 write new data to array of storage devices 410 of FIG. 4, the data is again striped across the storage devices... the data blocks B(0) through B(3) and P(3) are stored across the storage devices such that the data and parity**

**blocks are not stored on the same device… to reconstruct data in the event of a device failure, the blocks of new data that comprise a data stripe may be stored in locations on different devices". (Page 4, Par. 0043-Page 5, Par. 0045; Figure 4 and related text) which comprises "round-robin" between devices. Furthermore, "Fig. 5C illustrates an embodiment of how storage controller 401 of Fig. 3 may periodically realign non-uniformly sized parity groups into default sized parity groups" (Page 5, Par. 0046)]**

"storing the <u>first</u> data block at the physical disk location; and storing a first indirect block in the storage pool, wherein the first indirect block comprises the data block location and the data block checksum" **[Talangala discloses this limitation as "An indirection map (e.g. block remapping table) matches virtual block addresses to physical block addresses. Block-level checksums may be provided in the indirection map" (Column 6, paragraph 0059 and Figure 6C)]**

**<u>A storage pool comprising:</u>**

**<u>A plurality of child blocks, wherein each of the plurality of child blocks comprises one selected from the group consisting of the fist data block and a first indirect block, wherein the indirect block references at least on of the plurality of child blocks; A parent block referencing at least one indirect block; and</u> a <u>storage pool allocator configured to store the parent block and plurality of child blocks in the storage pool using a dynamic striping policy,</u> [Talagala discloses "an indirection map (e.g., block remapping table) matches virtual block address to physical block address. Block-level checksums may be provided in the indirection map" (Page 6, Par. 0059 and Figure 6C); "each valid PGT entry also includes a back pointer to the next entry in a parity group so that the first physical segment**

**in a parity group is linked to a second physical segment in that parity group, and the second physical segment to the third an so on, until the last physical segment contains the parity data for that parity group. The physical segment that contains the parity data in linked back to the first physical segment in the parity group, thereby creating a circular list for that parity group" (Page 6, Par. 0056; Figure 6 and related text); ["Storage Controller 401" (Figures 2 and 3 and Column 3, paragraph 0033)]**

**"changing the dynamic striping policy to obtain an updated dynamic striping policy; and storing a second data block using the updated dynamic striping policy [ With respect to this limitation, Talagala discloses "dynamic striping may be employed so that new writes form new parity groups. Thus, stripes of various sizes may be supported by the storage system" (Page 2, Par. 0012); therefore, updating the dynamic striping policy for new writes].**

Talagala does not specifically disclose the details having dynamic striping based on physical disk speed, free space available on physical disks, load on physical disks, and a round robin policy.

To further support Talagala, Lu explicitly discloses updating a striping/storage policy as **[a system and method for optimizing storage operations in which "an archive manager is a computer program that manages archive operations, such as creating and updating a storage policy, and retrieving data related to a storage policy... details of storage policies, such as the copy name, data stream, media group, combine data stream properties, etc." (Page 4, Par. 0046)].**

Dalal explicitly discloses a dynamic striping policy comprising at least one of a dynamic striping policy based on physical disk speed, free space available on physical disks, load on

physical disks, and a round robin policy as [**"Allocation coordinator 1010 obtains data form configuration database 1004, which includes data about templates, capabilities, rules and policy database 1006, which contains information about storage environment policies. An example of a policy is a specification of a stripe unit width for creating columns in a striped virtual object" and explains that "allocation coordinator 1010 also obtains information about the available storage environment from storage information collector" (Column 6, paragraph 0102 and Column 12, paragraph 0187) as having rules to allocate storage based on available storage space. Dalal also teaches that "striped storage has capacity, maximum bandwidth, and maximum I/O rate that is the sum of the corresponding values of its constituent disks" (Columns 13-14, paragraph 0213) wherein "optimum stripe unit size must be determined on a case-by-case basis, taking into account access patterns presented by the applications that will use striped storage" (Column 14, paragraph 0215) as taking into account, storage capacity, bandwidth and I/O rate to stripe storage devices**].

Talangala et al. (US 2002/0161972), Dalal et al. (US 2004/0123063) and Lu et al. (Us 2004/0225834) are analogous art because they are from the same field of endeavor of computer memory access and control.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the dynamic striping system as taught by Talangala, update a storage/striping policy as taught by Lu, and further stripe storage devices by selecting rules as taught by Dalal.

The motivation for doing so would have been because Dalal teaches that using certain rules to stripe a storage device [**"enable the device to provide certain capabilities, such as high performance, inherently" and explains that "to ensure that logical volume meets user**

**requirements, a combination of physical characteristics of some storage devices and software configuration of other storage devices using rules can be used to provide all capabilities meeting the user requirements" (Column 6, paragraph 0100)]** and Lu teaches updating of striping/storage policies is done for **["increasing the efficiency of storage management systems" (Page 2, Par. 0020)]**.

Therefore, it would have been obvious to combine Talangala et al. (US 2002/0161972) with Dalal et al. (US 2004/0123063) and Lu et al. (Us 2004/0225834) and for the benefit of creating a system/method for dynamic striping to obtain the invention as specified in claims 1 and 21.

4. As per **claim 2**, the combination of Talagala, Lu and Dalal discloses "The method of claim 1," **[See rejection to claim 1 above]** "further comprising: retrieving the **first** data block using the first indirect block" **[With respect to this limitation, Talangala disclose that "when a block read is requested, the block's indirection map entry is read to find the block's physical address" (Column 7, paragraph 0061, lines 8-10)]**.

5. As per **claim 3**, the combination of Talagala, Lu and Dalal discloses "The method of claim 1," **[See rejection to claim 1 above]** "further comprising: assembling the first indirect block, wherein assembling the first indirect block comprises populating a block pointer" **[Talangala discloses this concept as "a hash indirection table (HIT)" which "maps virtual block addresses to an entry or index number in a parity group table" (Column 6, paragraphs 0054-0055 and Figures 6B, 7A, 8A, 6C, 7B and 8B). Note that each virtual address in "HIT" maps to an entry in "PGT (parity group table)" and that each field in PGT table stores configuration information for each "indirect block"]**.

6. As per **claim 4**, the combination of Talagala, Lu and Dalal discloses "The method of claim 3," **[See rejection to claim 3 above]** "wherein populating the block pointer comprises: storing the **first** data block checksum in a checksum field within the block pointer;" **[Talangala discloses this concept as "each block's checksum is stored in an entry in the indirection map, e.g. as part of a block remapping table entry (e.g. PGT entry) for each block" (Column 6, paragraph 0058, lines 4-6 and Figures 6C, 7B and 8B) wherein each entry representing/pointing to a block in PGT contains a checksum in a checksum field]** "and storing the **first** data block location in the block pointer, wherein storing the data block location comprises storing a metaslab ID" **[Talangala discloses this concept as "the indirection map may also include a parity group pointer for each data block that points to a next member of that parity group" (Page 2, Par. 0013) wherein "when a READ or WRITE command is received for a block(s), the appropriate PGT entry is accessed to locate the blocks in the disk drives" (Page 6, Par. 0058) "HIT (Hash Indirection Table)" and explains having "PGT (Parity Group Table)" indices to access a PGT which contains configuration information for each of the parity groups such as a segment field which indicated the physical disk location (disk and segment) of parity groups (Column 6, paragraphs 0055, 0058, 0059 and Figures 6B, 6C, 7A, 7B, 8A and 8B). Talangala provides an example in which Virtual address 0 corresponds to PGT index 12, which contains valid data at physical segment D1.132 wherein "this may be interpreted as Disk 1, segment 132" (Column 6, paragraph 0057 and Figures 6B, 6C, 7A, 7B, 8A and 8B). As defined by Applicant, metaslabs are "contiguous regions of data" in which "the storage space in the storage pool is divided" (Specification, Par. 0031); therefore, Applicant should note that**

**these metaslabs may comprise any amount of contiguous data, such as segments or blocks into which a storage pool is divided, as described by Talagala]**

"and offset" **[Talangala discloses this concept as entries stored under the "Next Entry In Parity Group" field in PGT (parity group table) which points to the next virtual block entry (Column 6, paragraph 0057 and Figures 6B, 6C, 7A, 7B, 8A and 8B)].**

7. As per **claim 5**, the combination of Talagala, Lu and Dalal discloses "The method of claim 4," **[See rejection to claim 4 above]** "further comprising: storing a birth value in a birth field within the block pointer" **[Talangala discloses this concept as an embodiment having a "HIT (hash indirection table) which maintains generational images" and explains that "the PGT index columns are now labeled version zero through version two, where version zero corresponds to the most current version and version two corresponds to the oldest version" (Column 7, paragraph 0065 and Figures 8A and 8B)].**

8. As per **claims 6 and 15**, the combination of Talagala, Lu and Dalal discloses "The method/system of claims 3 and 13," **[See rejection to claim 3 and 13 above]** "wherein the first indirect block is assembled using a data management unit" **[With respect to this limitation, Talangala discloses "Storage Controller 401" (Figures 2 and 3 and Column 3, paragraph 0033)].**

9. As per **claims 7 and 17**, the combination of Talagala, Lu and Dalal discloses "The method/system of claims 1 and 13," **[See rejection to claims 1 and 13 above]** "wherein the storage pool comprises at least one storage device" **[With respect to this limitation, Talangala discloses "Array of Storage Devices 410" (Figures 2 and 3)].**

10. As per **claims 8 and 18**, Talangala discloses "The method/sytem of claims 1 and 13," **[See rejection to claims 1 and 13 above]** "wherein the storage pool is divided into a plurality of metaslabs" **[With respect to this limitation, Talangala discloses having different "stripes of data" within an array storage devices (Figure 4 and Column 4, paragraph 0043) and explains that a "stripe" of data is analogous to a "parity group" (Column 7, paragraph 0063, lines 10-11) wherein configuration information for each of the "parity groups" is stored in a "PGT (parity group table)" (Figures 6C, 7B and 8B) and further explains "the indirection map may also include a parity group pointer for each data block that points to a next member of that parity group" (Page 2, Par. 0013) wherein "when a READ or WRITE command is received for a block(s), the appropriate PGT entry is accessed to locate the blocks in the disk drives" (Page 6, Par. 0058). As defined by Applicant, metaslabs are "contiguous regions of data" in which "the storage space in the storage pool is divided" (Specification, Par. 0031); therefore, Applicant should note that these metaslabs may comprise any amount of contiguous data, such as segments or blocks into which a storage pool is divided, as described by Talagala]**.

11. As per **claims 9 and 19**, the combination of Talagala, Lu and Dalal discloses "The method/system of claims 8 and 18," **[See rejection to claims 8 and 18 above]** "wherein each of the plurality of metaslabs is associated with a metaslab ID" **[Talangala discloses this concept as each virtual block has a virtual address which is used to access a "HIT (Hash Indirection Table)" which contains "PGT (Parity Group Table)" indices to access a PGT which contains configuration information for each of the parity groups such as a segment field**

**which indicated the physical disk location (disk and segment) of parity groups (Column 6, paragraphs 0055, 0058, 0059 and Figures 6B, 6C, 7A, 7B, 8A and 8B)].**

12. As per **claims 10 and 20**, the combination of Talagala, Lu and Dalal discloses "The method of claims 9 and 19," **[See rejection to claims 9 and 19 above]** "wherein the data block location comprises the metaslab ID and an offset" **[Talangala discloses this concept as "the indirection map may also include a parity group pointer for each data block that points to a next member of that parity group" (Page 2, Par. 0013) wherein "when a READ or WRITE command is received for a block(s), the appropriate PGT entry is accessed to locate the blocks in the disk drives" (Page 6, Par. 0058) "HIT (Hash Indirection Table)" and explains having "PGT (Parity Group Table)" indices to access a PGT which contains configuration information for each of the parity groups such as a segment field which indicated the physical disk location (disk and segment) of parity groups (Column 6, paragraphs 0055, 0058, 0059 and Figures 6B, 6C, 7A, 7B, 8A and 8B). Talangala provides an example in which Virtual address 0 corresponds to PGT index 12, which contains valid data at physical segment D1.132 wherein "this may be interpreted as Disk 1, segment 132" (Column 6, paragraph 0057 and Figures 6B, 6C, 7A, 7B, 8A and 8B). As defined by Applicant, metaslabs are "contiguous regions of data" in which "the storage space in the storage pool is divided" (Specification, Par. 0031); therefore, Applicant should note that these metaslabs may comprise any amount of contiguous data, such as segments or blocks into which a storage pool is divided, as described by Talagala]**

"and offset" **[Talangala discloses this concept as entries stored under the "Next Entry In Parity Group" field in PGT (parity group table) which points to the next virtual block entry (Column 6, paragraph 0057 and Figures 6B, 6C, 7A, 7B, 8A and 8B)]**

13. As per **claim 11**, the combination of Talagala, Lu and Dalal discloses "The method of claim 1," **[See rejection to claim 1 above]** "wherein storing the **first** data block comprises using a storage pool allocator" **[With respect to this limitation, Talangala discloses "Storage Controller 401" (Figures 2 and 3 and Column 3, paragraph 0033)]**.

14. As per **claim 14**, the combination of Talagala, Lu and Dalal discloses "The system of claim 13," **[See rejection to claim 13 above]** "further comprising: a second indirect block, comprising a first indirect block checksum and a first indirect block location, wherein the storage pool allocator is further configured to store the second indirect block in the storage pool" **[With respect to this limitation, Talangala discloses writing a block having a checksum and a location in PGT (Parity Group Table) which have a "segment" field to store a location and a "checksum" field to store a checksum (Column 6, paragraph 0059 and Figures 6C, 7B and 8B) and provides (Figures 6C, 7B and 8B) which contain parity/stripe group tables having entries for multiple blocks of data stored in a storage pool]**.

15. As per **claim 16**, the system of claims 13, wherein the dynamic striping policy comprises at least one selected from the group consisting of a dynamic striping policy based on physical disk speed, a dynamic striping policy based on free space available on physical disks, a dynamic striping policy based on physical disks, and a round robin policy **[The rationale in the rejection to claims 1 and 21 is herein incorporated]**.

## II. ACKNOWLEDGMENT OF ISSUES RAISED BY THE APPLICANT

***Response to Amendment***

2. Applicant's arguments filed October 31, 2006 have been fully considered and are not persuasive.

3. As required by **M.P.E.P. § 707.07(f)**, a response to these arguments appears below.

### a. ARGUMENTS CONCERNING FORMAL MATTERS

4. The applicant's traversal of the formal requirements requested by the examiner are addressed in the following section as required by **M.P.E.P. § 707.07(f)**.

## III. ARGUMENTS CONCERNING PRIOR ART REJECTIONS

5. Claims must be given the broadest reasonable interpretation during examination and limitations appearing in the specification but not recited in the claim are not read into the claim (See M.P.E.P. 2111 [R-1]).

**1st POINT OF ARGUMENT**:

- Regarding the applicant's remarks that Talagala does not disclose a "hierarchical tree structure" as Talagala discloses a circular linked list; it is the Examiner's position that this limitation is not found within the scope of the claim language as claims 13 and 22 recite "the indirect block references **at least one** of the plurality of child blocks… a parent block referencing **at least one indirect block**… the parent block and the plurality of child blocks" **[Talagala discloses this limitation as "an indirection map (e.g., block remapping table) matches virtual block address to physical block address. Block-level checksums may be provided in the indirection map" (Page 6, Par. 0059 and Figure 6C); "each valid PGT entry also includes a back pointer to the next entry in a parity group so that the first physical segment in a parity group is linked to a second physical segment in that parity group, and**

**the second physical segment to the third an so on, until the last physical segment contains the parity data for that parity group. The physical segment that contains the parity data in linked back to the first physical segment in the parity group, thereby creating a circular list for that parity group" (Page 6, Par. 0056; Figure 6 and related text); ["Storage Controller 401" (Figures 2 and 3 and Column 3, paragraph 0033).** Applicant should note that a circular linked list will comprise "a first physical segment in a parity group" which comprises a parent block, **at least** one child linked to this parent block, and a plurality of child blocks as "second, third physical segments and so on"; as claimed by Applicant.

2nd POINT OF ARGUMENT:

6. Regarding Applicant's remarks that Talagala does not disclose metaslabs, it is the Examiner's position that Talagala discloses this limitiaon as [**As defined by Applicant, metaslabs are "contiguous regions of data" in which "the storage space in the storage pool is divided" (Specification, Par. 0031); therefore, Applicant should note that these metaslabs may comprise any amount of contiguous data, such as segments or blocks into which a storage pool is divided, as described by Talagala. Note that Talagala discloses "stripes of data" within an array storage devices (Figure 4 and Column 4, paragraph 0043) and explains that a "stripe" of data is analogous to a "parity group" (Column 7, paragraph 0063, lines 10-11) wherein configuration information for each of the "parity groups" is stored in a "PGT (parity group table)" (Figures 6C, 7B and 8B) and further explains "the indirection map may also include a parity group pointer for each data block that points to a next member of that parity group" (Page 2, Par. 0013) wherein "when a READ or WRITE command is received for a block(s), the appropriate PGT entry is accessed to locate the blocks in the disk drives" (Page 6, Par. 0058)].**

3rd POINT OF ARGUMENT:

7. Regarding Applicant's remark that Dalal does not disclose dynamic striping because after the creating of the logical disks, the striping is never changed again; Applicant is referred to the rejection of claims 1, 13 and 21-22 above wherein **[Talangala discloses that "With dynamic striping, the host machine interacts with the storage array via virtual addresses" and explains that "When a block is written, a physical location is chosen for it" (Column 6, paragraph 0059)Talagala also explains "when processor 100 of FIG. 1 write new data to array of storage devices 410 of FIG. 4, the data is again striped across the storage devices... the data blocks B(0) through B(3) and P(3) are stored across the storage devices such that the data and parity blocks are not stored on the same device... to reconstruct data in the event of a device failure, the blocks of new data that comprise a data stripe may be stored in locations on different devices" (Page 4, Par. 0043-Page 5, Par. 0045; Figure 4 and related text)] as disclosing a dynamic striping policy**. The reference to Dalal is merely used to illustrate different types of striping policies/algorithms/rules.

8. All arguments by the applicant are believed to be covered in the body of the office action or in the above remarks and thus, this action constitutes a complete response to the issues raised in the remarks dated October 31, 2006.

## IV. CLOSING COMMENTS

*Examiner's Note*

9. Examiner has cited particular columns and line numbers in the references as applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings in the art and are applied to the specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant, in preparing the responses, to fully consider the references in entirety as potentially

teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the examiner.

### *Conclusion*

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire three months from the mailing data of this action. In the event a first reply is filed within **two months** of the mailing date of this final action and the advisory action is not mailed until after the end of the **three-month** shortened statutory period, then the shortened statutory period will expire on the data the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing data of the advisory action. In no event, however, will the statutory period for reply expire later than **six months** from the mailing date of the final action.

## V. STATUS OF CLAIMS IN THE APPLICATION

11. The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. § 707.07(i)**:

### a(1) CLAIMS REJECTED IN THE APPLICATION

12. Per the instant office action, **claims 1-11 and 13-22** have received a second action on the merits and are subject of a final rejection.

### a(2) CLAIMS NO LONGER IN THE APPLICATION

13. Claim 12 was cancelled by amendment dated 10/31/2006.

14. For at least the above reasons it is the examiner's position that the applicant's claims are not in condition for allowance.

## VI. DIRECTION OF ALL FUTURE REMARKS

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yaima Campos whose telephone number is (571) 272-1232. The examiner can normally be reached on Monday to Friday 8:30 AM to 5:00 PM.

## IMPORTANT NOTE

16. If attempts to reach the above noted Examiner by telephone are unsuccessful, the Examiner's supervisor, Mr. Sanjiv Shah, can be reached at the following telephone number: Area Code (571) 272-4098.

17. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

January 10, 2007

SANJIV SHAH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

Yaima Campos
Examiner
Art Unit 2185